



10/657 964

Coff
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Sriram Satakopan et al.

Assignee: Sun Microsystems, Inc.

Title: LOW THRESHOLD VOLTAGE TRANSISTOR DISPLACEMENT IN A SEMICONDUCTOR DEVICE

Patent No.: 7,032,200

Issued: April 18, 2006

Atty. Docket No.: 004-8841

June 9, 2006

ATTN: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT –
PTO MISTAKE (37 C.F.R. § 1.322(a))**

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto is Form PTO/SB/44 (PTO-1050) suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file:
Application as filed, page 6, line 16 (headings in Table 2);
Response to Non-Final Office action filed October 19, 2005, page 6, lines 14, 20, and 21 of Claim 20;
Response to Non-Final Office action filed October 19, 2005, page 7, line 3 of Claim 23.
3. Please send the Certificate to:

Nicole Teitler Cave
ZAGORIN O'BRIEN GRAHAM LLP
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AUSTIN, TEXAS 78731-1191

*Certificate
JUN 15 2006
of Correction*

Respectfully submitted,



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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,032,200

DATED : April 18, 2006

INVENTOR(S) : Sriram Satakopan et al.

It is certified that error(s) appear(s) in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, Table 2, replace "Path cycle time without LV_t device penalty" with --Path cycle time without LV_t device--;

In column 7, line 20, replace "rate" with --gate--;

line 29, replace "Particular low threshold variant of a Rate" with --particular low threshold variant of a gate--;

In column 8, line 11, remove the comma after "files".

MAILING ADDRESS OF SENDER:

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PATENT NO. 7,032,200